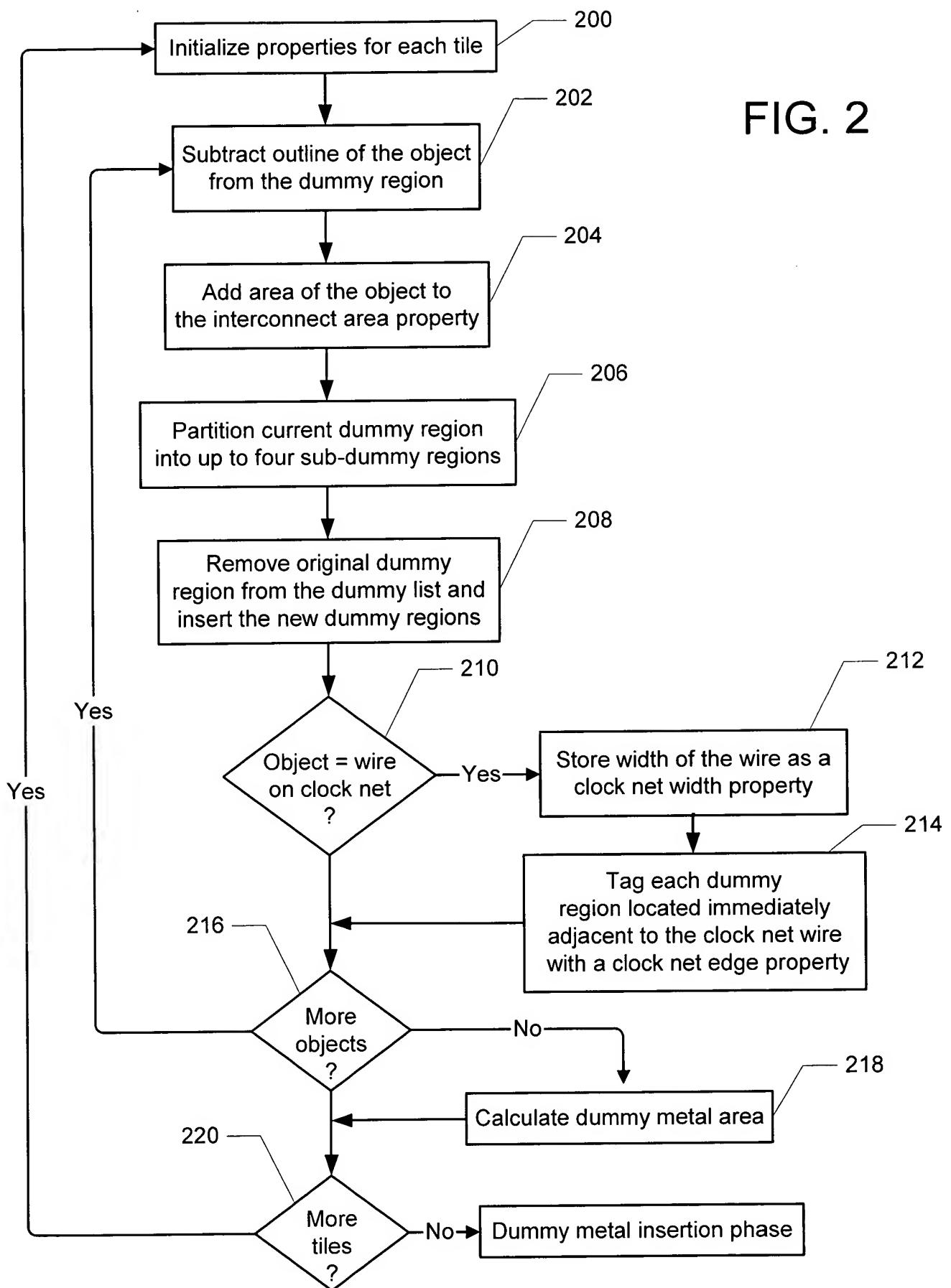


FIG. 1

FIG. 2



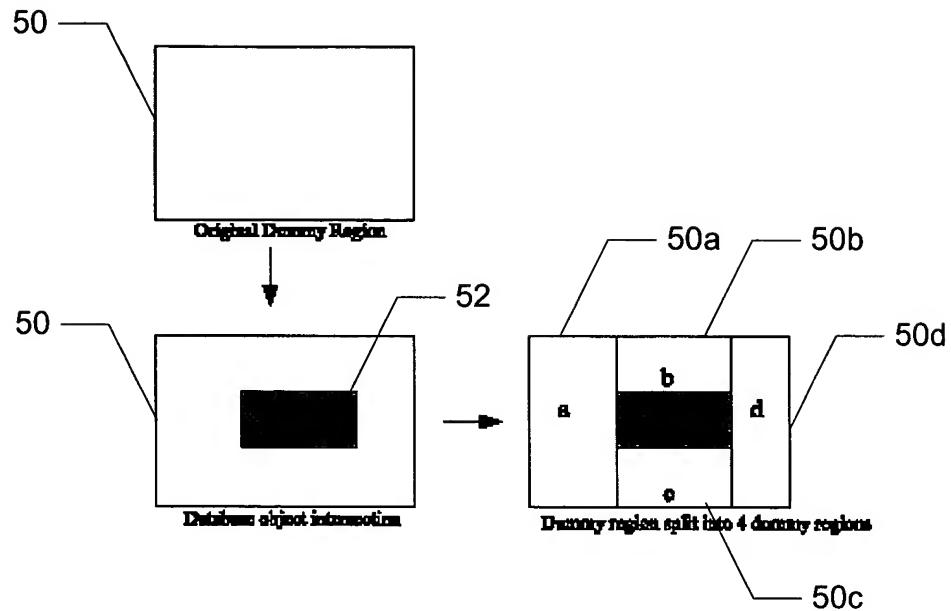


FIG. 3

Tile Properties

| Dummy List 60 | | | |
|---------------|-----------------|-------------------|------------------|
| Dummy Region | Clock Net Width | Clock Net Edge | Timing Factor |
| Dummy Region | | | Timing Factor |
| Dummy Region | Clock Net Width | Clock Net Edge | Timing Factor |
| Dummy Region | | | Timing Factor |
| Dummy Region | Clock Net Width | Clock Net Edge | Timing Factor |
| | | | |
| 50 | 68 | 70 | 72 |
| Dummy Region | Clock Net Width | Clock Net Edge | Timing Factor |
| | | | |
| Tile Area | | Interconnect Area | |
| 62 | 64 | 66 | Dummy Metal Area |

FIG. 4

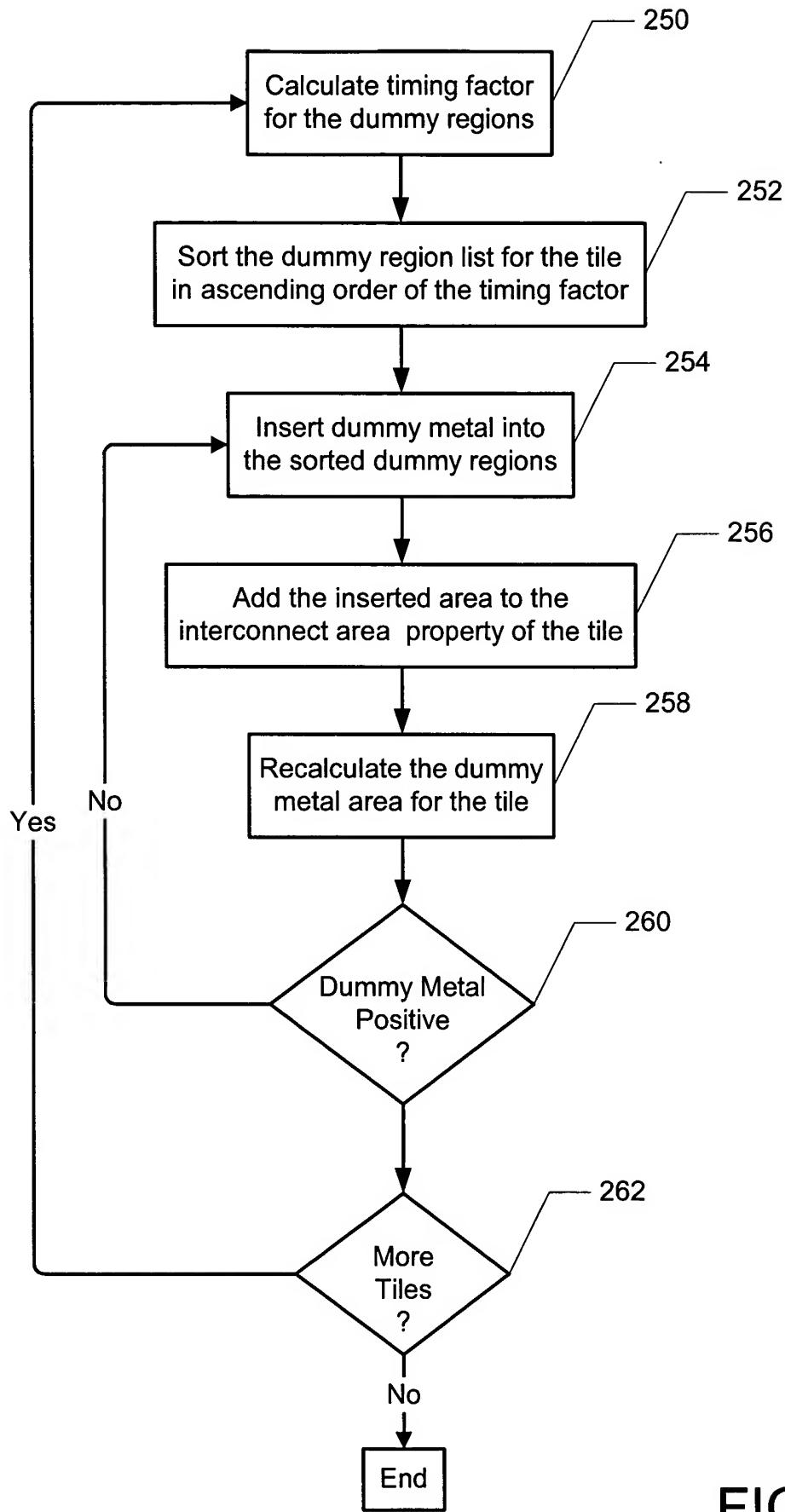


FIG. 5

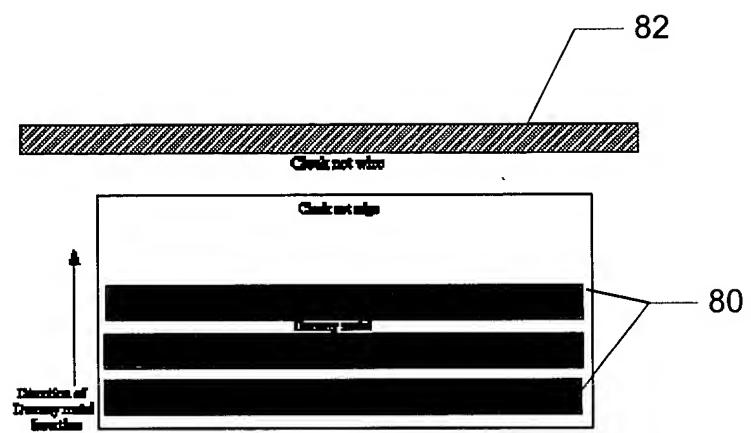


FIG. 6